REMARKS

Please reconsider this application in view of the above amendments and the following remarks.

- Claims 1-6 and 15-22 are pending.
- Claims 1-14 are rejected.
- Claims 15-22 are newly added.

Claim 1 has been amended to clarify the claimed invention. Namely, the structure previously called a barrier is now called a "pore sealing layer." Support for this amendment can be found in the specification, as filed, at page 6, lines 11 through 16. Additionally, claims depending from claim 1 have been amended to make their language parallel that of the amended language in claim 1.

Claim 15 is newly added; support for it can be found in the specification, as filed, at page 7, lines 1 and 3.

Claim 16 is newly added. It adds a barrier element to the device. This barrier element is a typical barrier element as is known in the art and as discussed on Page 1, line 20, of the specification, as filed.

Claims 17 and 18 are newly added. Support for these claims can be found in the specfication as filed, page 6, lines 17-20.

Claim 19 is newly added. Support for incomplete pore sealing and its solution can be found in the specification as filed, page 6, lines 8-10.

Claims 20-22 are drawn to methods of making the integrated circuit of claim 1. They are commensurate in scope with the claimed integrated circuits and are proper once the device claims are found allowable. At this point, these claims are also withdrawn from examination pending the allowance of a device claim. Support for these claims can be found in the specification as filed at page 6-7.

Finally, some claims have been reformatted.

Background

As the size of integrated circuits becomes smaller, the size of the individual devices, conductors, and interconnects must decrease in size. As the size of the conductor decreases, the delay time caused by charging and discharging the conductor becomes larger. This delay time is related to conductor resistance multiplied by conductor capacitance and results in slower chip speeds.

One tool for reducing the delay time is to use lower K dielectrics, but using standard non-porous dielectrics limits how much lower the dielectric constant can be made. One current technique for reducing the dielectric constant is to mix air or gas into the dielectric material in the form of gas bubbles in the material. But when the gas bubble inclusions broach the dielectric material's surface, they become cavities or pores in the surface. See Figure 1 of this response. These pores are typically covered by the barrier layer used for segregating the conductor material from the dielectric material forming the conductor channels. Yet, the barrier layer must become smaller as the size of the device becomes smaller. Eventually, the barrier layer becomes thin enough that it cannot fill or cover the pores in the dielectric. Having open pores allows the conductor to fill or enter the pores thereby defeating the function of the barrier layer. This problem is known in the art.

The current invention uses a pore sealing layer under the barrier layer to cover or fill the pores before the barrier layer is applied. See Figure 2 in this response. In some embodiments, the process comprises depositing a first material and a second material onto the sidewalls and the floor of the trench. But the initial deposition may not seal the discontinuities in the sidewalls because the low k dielectric sidewalls are particularly porous. So, to create a better seal, energy is applied to the materials deposited on the sidewalls and the floor of the trench. This causes the deposited materials to react to form a compound in which the grain growth or local atom movement seals pores in the dielectric and fills in the dielectric sidewalls. The heat-treated material is referred to in this application as a "pore sealing layer."

After the pore sealing layer is constructed, a standard barrier layer may be applied.

Art-based rejections

The examiner has rejected claims 1-4 under 35 USC §102(b) as being anticipated by Rideout, U. S. Patent No. 4,075,045, D1.

As amended, applicant's claim 1 recites a "pore sealing layer." D1, apparently, does not teach such a layer. Therefore, D1 does not anticipate claim 1. Please remove this rejection.

Claims 2-4 depend from claim 1 and, therefore, contain all of the limitations of claim 1. This means that claims 2-4 each are patentable over D1 because of the "pore sealing layer" limitation described above. Please remove this rejection of claims 2-4.

Furthermore, the claim amendment makes the additional discussion in this section moot. Because of this, applicant chooses not to address the remainder of the Examiner's discussion in this section now. But should such a duty arise in the future, applicant reserves the right to address the discussion then. Applicant specifically does not acquiesce to the facts, assumed facts, or reasoning contained in this section.

The examiner has rejected claims 1-6 under 35 USC §102(e) as being anticipated by Lopatin, U. S. Patent No. 6,420,189 (D2).

As amended, applicant's claim 1 recites a "pore sealing layer." D2, apparently, does not teach such a layer. Therefore, D2 does not anticipate claim 1. Please remove this rejection.

Claims 2-6 depend from claim 1 and, therefore, contain all of the limitations of claim 1. This means that claims 2-6 each are patentable over D2 because of the "pore sealing layer" limitation described above. Please remove this rejection of claims 2-6.

Furthermore, the claim amendment makes the additional discussion in this section moot. Because of this, applicant chooses not to address the remainder of the Examiner's discussion in this section now. But should such a duty arise in the future, applicant reserves the right to address the discussion then. Applicant specifically does not acquiesce to the facts, assumed facts, or reasoning contained in this section.

The examiner has rejected claims 7, 8, 10, 13, and 14 under 35 USC §102(b) as being anticipated by Dubin et al., U. S. Patent No. 5,695,810 (D3).

As amended, applicant's claim 7 recites a "pore sealing layer." D3 does not teach such a layer. Therefore, D3 does not anticipate claim 1. Please remove this rejection.

Claims 8, 10, 13, and 14 depend from claim 7 and, therefore, contain all of the limitations of claim 7. This means that claims 8, 10, 13, and 14 each are patentable over D3 at least because of the "pore sealing layer" limitation described above. Please remove this rejection of claims 8, 10, 13, and 14.

Furthermore, the claim amendment makes the additional discussion in this section moot. Because of this, applicant chooses not to address the remainder of the Examiner's discussion in this section now. But should such a duty arise in the future, applicant reserves the right to address the discussion then. Applicant specifically does not acquiesce to the facts, assumed facts, or reasoning contained in this section.

The examiner has rejected claims 7-9 and 11-14 under 35 USC §102(e) as being anticipated by Leu et al., U. S. Patent No. 6,605,874 (D4).

As amended, applicant's claim 7 recites a "pore sealing layer." D4 does not teach such a layer. Therefore, D4 does not anticipate claim 1. Please remove this rejection.

Claims 8-9 and 11-14 depend from claim 7 and, therefore, contain all of the limitations of claim 7. This means that claims 8-9 and 11-14 each are patentable over D4 at least because of the "pore sealing layer" limitation described above. Please remove this rejection of claims 8-9 and 11-14.

Furthermore, the claim amendment makes the additional discussion in this section moot. Because of this, applicant chooses not to address the remainder of the Examiner's discussion in this section now. But should such a duty arise in the future, applicant reserves the right to address the discussion then. Applicant specifically does not acquiesce to the facts, assumed facts, or reasoning contained in this section.

Since all claims are in a condition for allowance, please issue a Notice of Allowability so stating. If I can be of any help, please contact me.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on Date: January 27, 2005 By: Patricia Gamble

Name of person signing certification